JNEST EISSN: 2961-8738 ● PISSN: 2961-8916 ● DOI: 10.56741/jnest.v5i02.2114
Article Received 1 March 2026, Revised 2 August 2026

Temperature-Stable 437.5 MHz Current-Starved Ring Oscillator with Bandgap Reference for Nanosatellite Beacon Transmitters

Thit Waso Khine*, Lei Lei Yin Win, Khin Kyu Kyu Win, Ei Ei Khin, Mya Mya Aye

***Abstract*—This paper presents a 437.5 MHz 3-stage CMOS current-starved ring oscillator (CSRO) with bandgap reference (BGR) design including process, voltage, and temperature (PVT) analysis. The circuit was designed and simulated in LTspice software using BSIM3 models, Level 8, 180 nm technology. The main objective is to design a simple, low-power, low-cost, high-temperature-stable (437 MHz) current-starved CMOS ring oscillator for a nanosatellite Morse code beacon transmitter. For practical implementation, the circuit was designed with standard E12 series resistor values, resulting in a final frequency of 437.5 MHz. The oscillator consumes 0.669 mW from a 1.8 V supply voltage, achieving phase noise of − 95.7 dBc/Hz at 1 MHz offset and a figure-of-merit (FOM) of −150.27. The CSRO exhibits a frequency variation of 1.31% over the temperature range of -40℃ to 125℃, demonstrating excellent robustness. A supply voltage variation of 5% results in 7.02 % of frequency change. In this work, a bandgap reference circuit (BGR) was separately designed and simulated, which gave the temperature coefficient of 10.68 ppm/℃ across the temperature of −40℃ to 125 ℃ and line regulation of ±0.18% across the supply voltage variation of 10%. The design includes PVT analysis across worst-case corners, temperature extreme and ±5% supply voltage variation on operating frequency and power consumption to ensure results closely match measurements.**

***Index Terms*—Bandgap Reference, Current-Starved Ring Oscillator, Low power CMOS, Nanosatellite Beacons, Phase Noise, PVT analysis, Temperature Coefficient**

I. Introduction

THE increasing demand for Earth observation and communication has led to the widespread use of Low Earth Orbit (LEO) nanosatellites. These satellites operate under strict power, volume, and thermal constraints. The frequency, 437 MHz is the internationally recognized frequency for nanosatellite beacons within 70 cm amateur band. Ring oscillators are attractive for nanosatellite applications because of their compact area, low power consumption, and ease of integration in standard CMOS technology. Among them, the current-starved ring oscillator (CSRO) offers additional controllability by regulating the inverter delay through bias current limitation, enabling frequency tuning without large passive components. Nevertheless, the oscillation frequency of a CSRO is highly sensitive to temperature, supply voltage, and process variations. To address this limitation, a temperature-compensated biasing approach is required [1]. A bandgap reference (BGR) circuit provides a near temperature-independent reference voltage. By using the bandgap reference to generate a stable bias current for the current-starved stages, the temperature dependence of the oscillation frequency can be significantly reduced. The block diagram of the proposed CSRO is shown in Fig. 1.

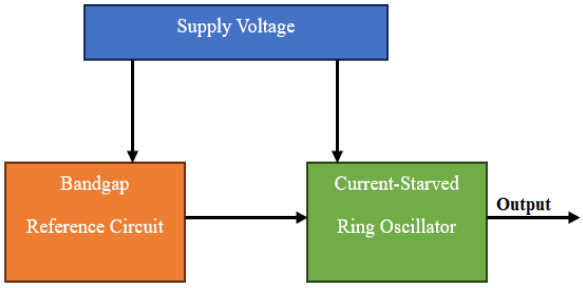


Fig. 1. Block diagram of the proposed CSRO.

The paper is organized as follows: Section II expresses the bandgap reference circuit design methdology and simulation results in LTspice. Section III mentions design methodology for current-starved ring oscillator with BGR and simulation results in LTspice. Section IV presents the PVT analysis of the proposed CSRO on the operation frequency and power. Section V concludes the study and results.

II. The Bandgap Reference Circuit Design Methodology

A bandgap reference circuit is one that provides temperature independent constant output voltage. It combines the proportional to absolute temperature (PTAT) that increase with temperature and complementary proportional to absolute temperature (CTAT) that decreases with temperature to reduce the temperature variation affects by using simple two BJTs. A bandgap voltage reference circuit is shown in Fig. 2 which is based on the circuit presented in [3].

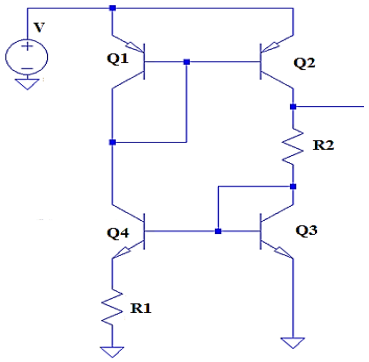


Fig. 2. Bandgap voltage reference circuit.

Thit Waso Khine (Corresponding author), **Lei Lei Yin Win**, **Khin Kyu Kyu Win**, **Ei Ei Khin,** and **Mya Mya Aye** are with the Department of Electronic Engineering, Yangon Technological University, Gyogone, Insein PO, 11011, Yangon, Myanmar. Correspondence: ecdepartment.ytu@gmail.com.

© 2026 IISTR

PTAT component is the voltage difference across two BJTs with different emitter areas (ΔV_{BE}) and CTAT is the base-emitter voltage (V_{BE}) of a BJT [2]. For this action, it is needed to set the same current for the two BJTs. It commonly has an output voltage of around 1.25V which is close to the theoretical 1.22eV energy gap or band gap of Silicon at absolute temperature [3]. The two PNP BJTs (Q_1 *and* Q_2) serve as a current mirror to supply the same current to the two NPN BJTs (Q_3 *and* Q_4) for having different current densities between them to produce bandgap voltage reference.

$$\Delta V_{BE} = V_{BE4} - V_{BE3} = V_T \ln(n). \quad (1)$$

$$V_{bgr} = V_{BE} + \frac{R_2}{R_1}\frac{KT}{q}\ln(n). \quad (2)$$

where n is the collector current ratio of the transistors.

In this BGR design, two 2N3904 NPN with an emitter area ratio of 8:1 is used to generate the PTAT voltage. This ratio is implemented in simulation by scaling the area parameter, which corresponds to paralleling eight transistors in practical implementation. Two 2N3906 PNP devices form a current mirror. This configuration produces ΔV_{BE} of approximately 54 mV at room temperature. Based on this area ratio, the resistors R_1 and R_2 are calculated to achieve first-order temperature compensation, with the final values selected by considering the power-area trade-off. After simulation in LTspice using supply voltage =1.8 V, R_1= 330 Ω, R_2= 3.3 kΩ, the circuit gives the output voltage (Vbgr) of 1.136 V at 27℃.

The BGR is simulated over the temperature range of -40℃ to 125℃, which is specifically chosen for nanosatellite applications where extreme thermal variations are encountered. The output voltage of bandgap reference (Vbgr) is 1.135 V at -40℃, 1.136 V at both 27℃ and 85℃, and 1.134 V at 125℃. Based on these measurements, the temperature coefficient (T_C) is calculated as in (3) [4], resulting 10.68 ppm/℃, which demonstrates outstanding thermal stability for space-based applications.

$$T_C = \frac{V_{max} - V_{min}}{V_{avg}(T_{max} - T_{min})} 10^6 \text{ ppm/℃}. \quad (3)$$

The first-order temperature compensation graph of the BGR is shown in Fig. 3.

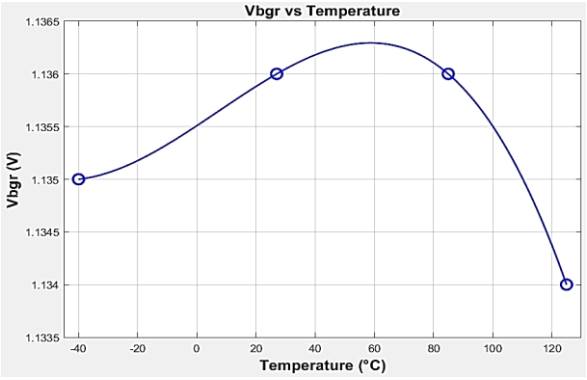


Fig. 3. First-order temperature compensation graph.

Similarity, the BGR is also simulated over the supply voltage of ±10% variation that is (1.62 V, 1.8 V and 1.98 V). This gives the results of only ±0.18% changes in the output voltage of BGR, demonstrating excellent supply rejection or line regulation which is shown in Fig. 4.

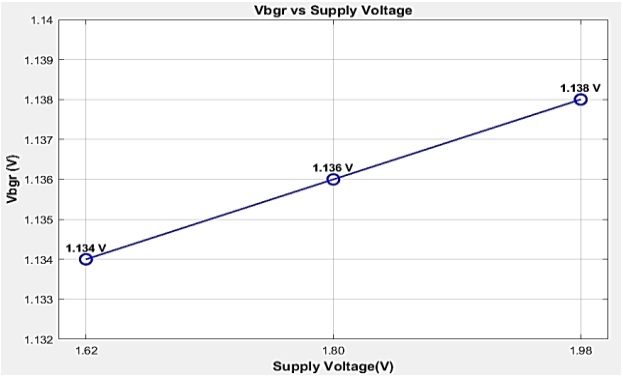


Fig. 4. Bandgap reference voltage vs supply voltage.

To maintain simplicity and minimize power consumption, only first-order compensation is employed. This bandgap reference circuit will be integrated with the current-starved CMOS ring oscillator. The comparison BGR results with previous works in the literature is as in I.

TABLE 1. COMPARISON BGR RESULTS WITH PREVIOUS WORKS IN THE LITERATURE

Methods	Supply voltage (V)	Output voltage (V)	Temperature range (℃)	Temperature Coefficient
[2]	1.8	0.235	-40 to 120	14.5 ppm/℃
[4]	1.8	1.251	-40 to125	3.74 ppm/℃
[5]	1.6 to 4.15	0.8-1-1.3	-55 to 130	13-44 ppm/℃
This work	1.8	1.136	-40 to 125	10.68 ppm/℃

III. DESIGN METHODOLOGY FOR CURRENT-STARVED RING OSCILLATOR WITH BGR

A. Conventional current-starved ring oscillator

A current-starved ring oscillator is a modified ring oscillator in which the current available to each inverter stage is intentionally limited by additional biasing transistors [6]. A CMOS 3-stages current-starved ring oscillator is shown in Fig. 5.

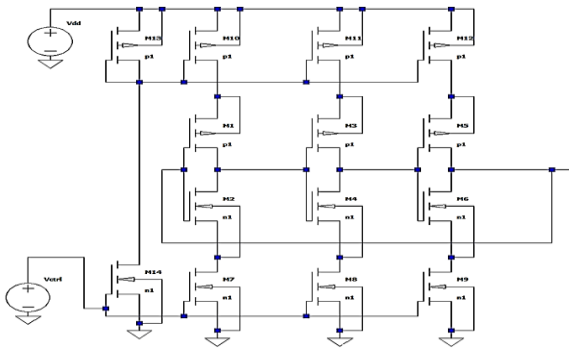


Fig. 5. CMOS 3-stage current-starved ring oscillator.

$$f_{osc} = \frac{1}{2N\,t_d}. \quad (4)$$

where N is number of inverter stages, f_{osc} is operating frequency and t_d is propagation delay per stage.

$$f_{osc} = \frac{I_d}{NC_{tot}V_{ctrl}}. \quad (5)$$

For the design of CSRO, there are four main steps (1) selecting W/L of PMOS and NMOS, (2) selecting number of stages, (3) selecting supply voltage and (4) selecting control voltage (V_{ctrl}) [6]. In this work, operating frequency is fixed at 437 MHz for nanosatellite beacons to select control voltage. Choosing W of all PMOS at 2 µm, W of all NMOS at 1µm and L of all PMOS and NMOS at 0.18 µm with supply voltage of 1.8 V, 3-stages, control voltage of 0.6133 V make the oscillator to oscillate at nearly 435 MHz. Although it gives nearly 437 MHz at normal temperature 27℃, large frequency deviations occur over −40℃ to 125℃ which is shown in Fig. 6.

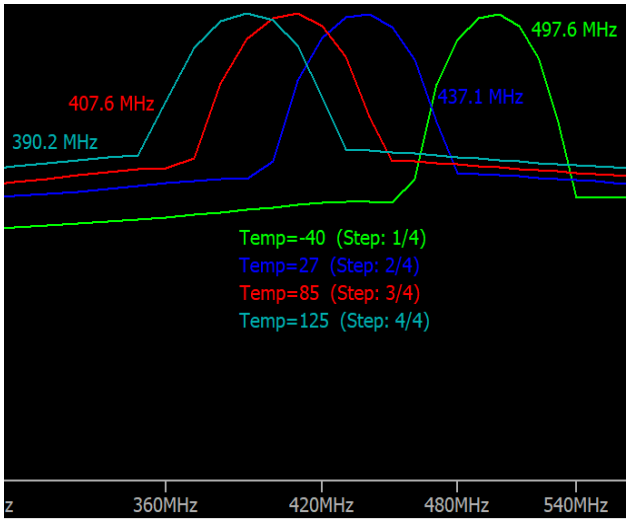


Fig. 6. Large frequency deviations of the CSRO.

This highlights the need for a temperature-independent control voltage. Therefore, the control voltage (Vctrl) must be connected to the bandgap reference circuit.

B. Combination of bandgap reference circuit and CMOS CSRO

To connect the BGR to the CSRO, a resistor with two NMOS current mirror is inserted between the BGR and the CSRO. The resistor value is calculated as in (6).

$$R = \frac{V_{bgr} - V_{ctrl}}{I_{bgr}}. \quad (6)$$

The calculated resistor value of 4.2 kΩ gave good temperature stability (4 MHz variation) but frequency is below 437 MHz. Increasing resistor value to 6.8 kΩ degraded temperature stability (12 MHz variation) without reaching 437 MHz. The optimum was achieved by increasing the CSRO current source PMOS(s) widths to 5 µm, yielding 437.5 MHz at 27℃ with 5.7 MHz frequency variation and power consumption is 0.669 mW. The proposed CSRO with the BGR using the standard resistors values is shown in Fig. 7.

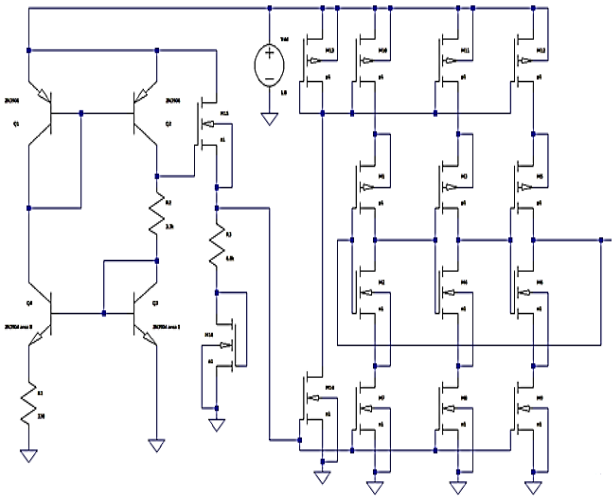


Fig. 7. The proposed CSRO with BGR.

Transient waveforms showing 437.5 MHz oscillation of the proposed CSRO is shown in Fig. 8.

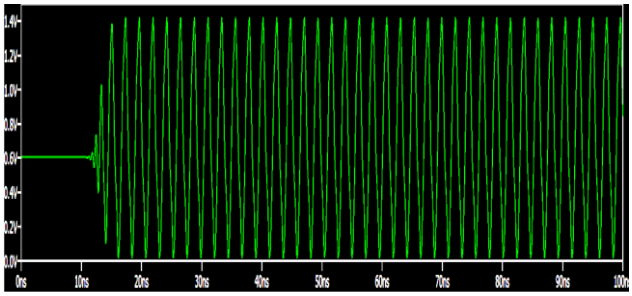


Fig. 8. Transient waveforms showing 437.5 MHz oscillation of the proposed CSRO.

This optimal design was obtained through analytical calculation combined with iterative simulation. From the Fast Fourier Transform (FFT) plot simulation result, the overall harmonic distortion yielded a value of 10.96% which is less than 13.82 % presented in [6]. Small frequency deviations of the proposed CSRO with BGR is as shown in Fig. 9.

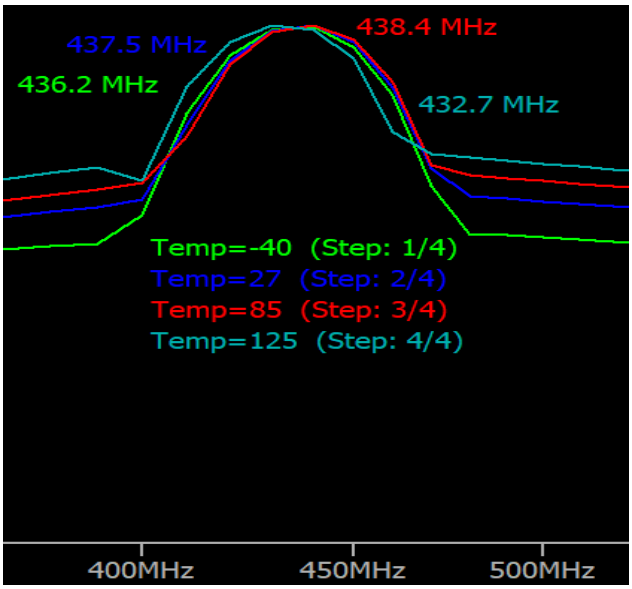


Fig. 9. Small frequency deviations of CSRO with BGR.

Phase noise is also approximated using FFT result in LTspice simulation at 27℃ at offset frequency of 1 MHz. From the approximation $P_{sideband}$ value at 438.5 MHz with the simulation time of 1 ms in FFT plot, phase noise is calculated as in (7), resulting -95.7 dBc/Hz demonstrating its suitability for precision frequency generation.

$$L\{\Delta\omega\} = 10 \log \left[\frac{P_{sideband}(\omega_o+\Delta\omega,1\ Hz)}{P_{carrier}}\right]. \quad (7)$$

where, ω_o is oscillation frequency and $\Delta\omega$ is offset frequency from ω_o [7].

Figure of merit (FOM) is calculated at 1 MHz offset as in (8) [8], resulting the value of -150.27.

$$FOM = \text{PN} - 20log\left(\frac{f_{osc}}{\Delta f}\right) + 10\log\left(\frac{P(mW)}{1mW}\right). \quad (8)$$

where PN is the phase noise at a particular frequency offset Δf .

IV. Process, Voltage, Temperature (PVT) Analysis for the Proposed CSRO With BGR

To evaluate the design's robustness, PVT analysis was performed on the operating frequency and power consumption at extreme corners.

A. *Temperature Variation Effects on Frequency and Power Consumption*

The CSRO demonstrates excellent frequency stability across the -40 ℃ to 85℃ temperature range, with a variation of only 0.5 %. At 125℃, a slight frequency drop to 432.7 MHz is observed, which can be caused due to the second-order curvature effects of the bandgap reference combined with the non-linearity of the CSRO at extreme temperatures. However, the total frequency variation from -40℃ to 125 ℃ is 5.7 MHz, which corresponds to a variation of only 1.31 % . This level of stability, achieved with a first-order compensated bandgap, is better than conventional CSRO. Temperature variation effects on frequency is shown in Fig. 10.

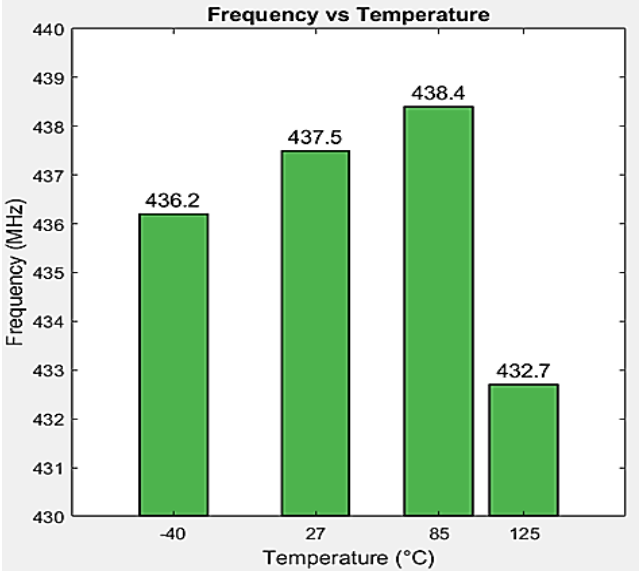


Fig. 10. Temperature variation effects on frequency.

The power consumption simply increases with temperature increases but even the power at the highest temperature of 125℃ is less than 0.9 mW which is as shown in Fig. 11.

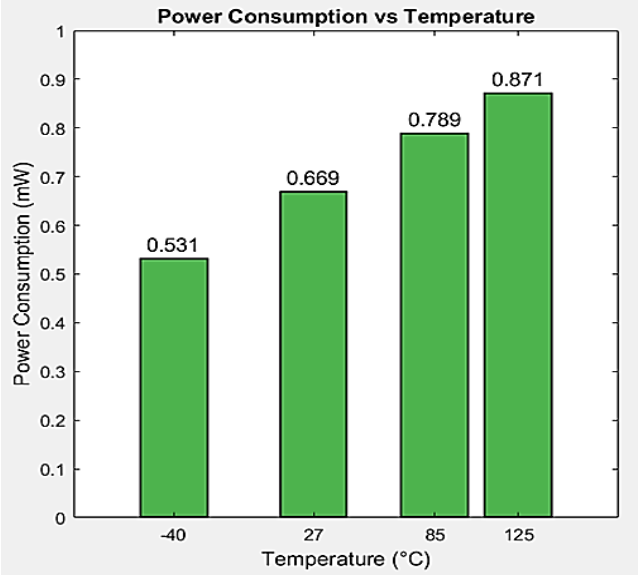


Fig. 11. Temperature variation effects on power.

B. *Supply Voltage Variation on Frequency and Power Consumption*

The bandgap reference itself operates well within ±10% supply voltage variation, but the integrated CSRO is limited to ±5% supply variation for acceptable frequency stability. The oscillator exhibits a frequency variation of 7.05 % over a ±5% change in supply voltage as shown in Fig. 12. While the design demonstrates excellent temperature stability, it shows moderate sensitivity to supply voltage variations. In future work, a low- dropout regulator (LDO) or voltage regulator could be integrated for higher supply immunity.

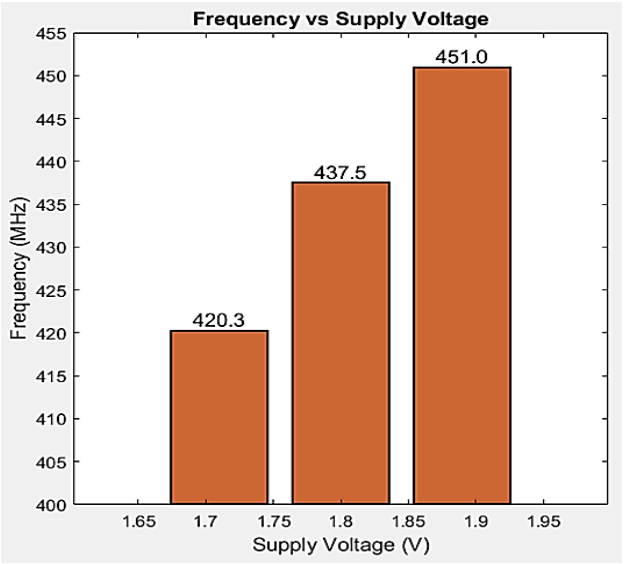


Fig. 12. Supply voltage variation effects on frequency.

The power consumption is the same manner as temperature effects but the power at the maximum voltage of 1.89 V is less than 0.8 mW as shown in Fig. 13.

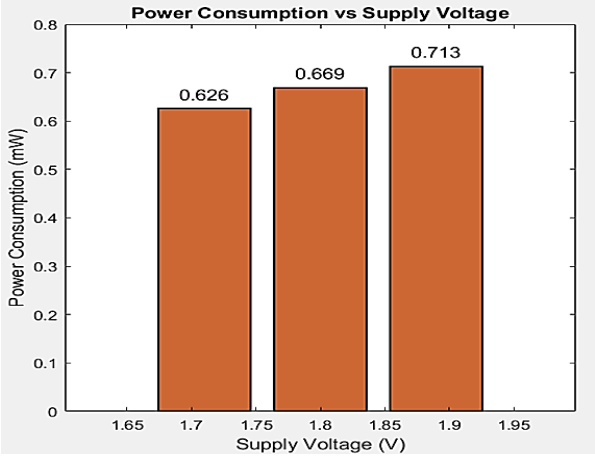


Fig. 13. Supply voltage variation effects on power.

C. Process Variation on Frequency and Power Consumption

The BSIM3 model was selected for this work due to its availability, LTspice compatibility, and sufficient accuracy for 437 MHz beacon applications. Its low-cost nature and mature status make it an ideal choice for academic research. For the process variation analysis, the three most influential parameters: threshold voltage (vth0), carrier mobility (u0) and gate-oxide thickness (tox) were varied manually in the model files according to the process corner [9]. The simulation covered five standard process corners: TT (typical-typical), FF (fast-fast), SS (slow-slow), SF (slow-fast) and FS (fast-slow) [10]. Process variation for NMOS and PMOS is as in Table II.

TABLE II. PROCESS VARIATION FOR NMOS AND PMOS

Parameter	TT	FF	SS	SF	FS
NMOS vth0	0.4	0.36	0.44	0.44	0.36
PMOS vth0	-0.4	-0.36	-0.44	-0.36	-0.44
Tox(µm)	4.0	3.8	4.2	4.2/3.8	3.8/4.2
NMOS u0	300	330	270	270	330
PMOS u0	100	110	90	110	90

Although the oscillator works across all five corners, it shows extreme sensitivity to process corners as shown in Fig. 14.

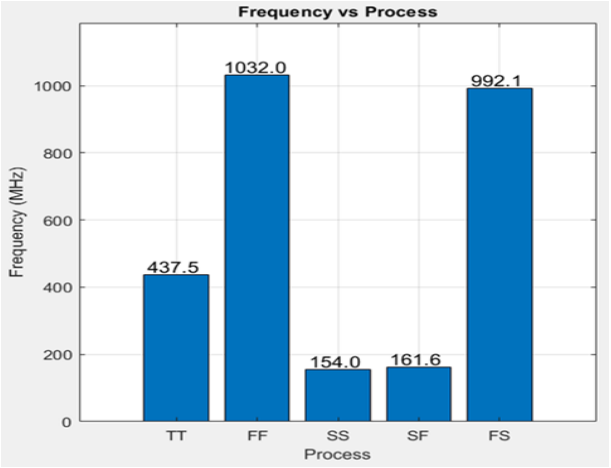


Fig. 14. Process variation effects on frequency.

However, the frequency at FF and FS falls within the UHF band (300 MHz to 3 GHz), but the SS and SF corners produce frequencies in the VHF range (30-300 MHz), falling outside the target UHF band. It indicates that the circuit is highly dependent on transistor threshold voltages and carrier mobilities. In future work, it requires additional process compensation techniques such as calibration circuits, process-tracking biasing or post-fabrication trimming for practical implementation in mass production.

As the power consumption, it is the highest in FF corner but is not more than 0.8 mW as shown in Fig.15.

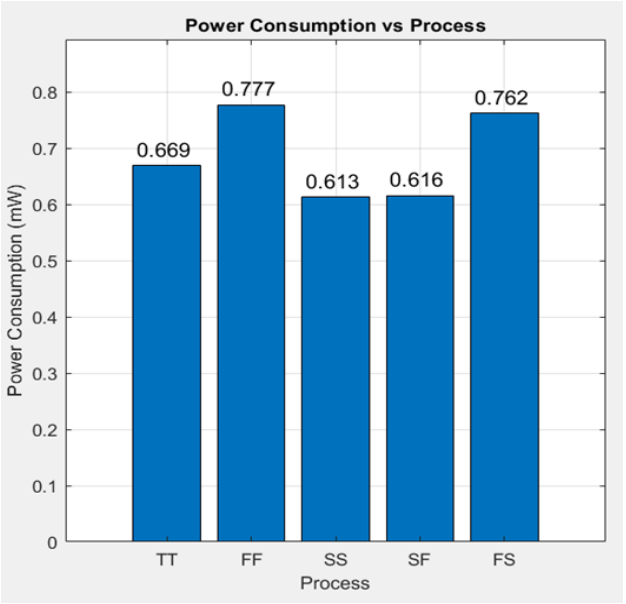


Fig. 15. Process variation effects on power.

Process variation analysis reveals limitations of the BSIM3 model. However, for the target application of nanosatellite beacon transmitters, which involve one-off or low-volume production runs, this process sensitivity can be mitigated through post-fabrication trimming or external component tuning.

For high-volume commercial applications, however, additional on-chip process compensation techniques would be required. The performance of the proposed CSRO at PVT variation is summarized in TT, FF and SS as in III.

TABLE III. PERFORMANCE OF THE PROPOSED CSRO AT PVT VARIATION

Corner	Supply voltage	Temperature	Frequency	Power (mW)
TT	1.8 V	27℃	437.5 MHz	0.669
FF	1.89 V	-40 ℃	1234.8 MHz	0.717
SS	1.71 V	125 ℃	194.6 MHz	0.775

Under nominal conditions, the proposed design offers a suitable solution for prototype applications.

A performance comparison between this work and previously published CSRO is presented in IV. All values are based on typical-typical (TT) process corner simulations at nominal conditions.

TABLE IV. PERFORMANCE COMPARISON BETWEEN THE PROPOSED CSRO AND PREVIOUSLY PUBLISHED CSRO

References	[11]	[12]	[12]	This work
Technology	90 nm	65 nm	180 nm	180 nm
Supply voltage (V)	1.2	1.2 V	1.8	1.8
Frequency	1.999 GHz	1.75 GHz	410 MHz	437.5 MHz
Phase noise at 1 MHz (dBc/Hz)	−86.67	−108.4	−373.3	−95.7
Power Consumption (µW)	348.48	1360	216	669
FOM	−157.25	171.89	196.21	−150.27

V. CONCLUSION

The proposed CSRO with BGR demonstrates excellent temperature stability. It exhibits moderate sensitivity to supply voltage variation. However, the design shows significant susceptibility to process variations, with frequency ranging from 154 MHz at SS corner to 1032 MHz at FF corner. The worst-case power consumption remains under the 1 mW threshold. Despite process variation limitation, under nominal TT corner conditions, it achieves the target frequency of 437.5 MHz with excellent temperature stability while consuming 0.669 mW of power. The design is ideal for low-volume production where per-device calibration is feasible. In conclusion, the proposed design is simple, less complexity and provides a solid foundation for nanosatellite missions which is low-volume applications, requiring low power and high temperature stability. Future work will focus on integrating this oscillator with a power amplifier, modulation circuitry and antenna interface to realize a fully functional beacon transmitter for nanosatellites.

ACKNOWLEDGMENT

The author would like to thank all the teachers from the Department of Electronic Engineering, Yangon Technological University, for their support, encouragement and invaluable guidance in the preparation of this paper. The author also wishes to give her thanks to all teachers who teach her in her whole life.

REFERENCES

[1] S. S. Pothuri, "Design of CMOS ring oscillator," M.Tech. project report, Dept. Elect. Eng., Indian Institute of Technology Madras, Chennai, India, Jun. 2022.

[2] X. Ran, M. Chen, W. Wang, L. Zhou, H. Wang, and J. Chen, "A CMOS bandgap reference based on switched capacitor with temperature compensation method," *IEICE Electronics Express*, vol. 19, no. 4, pp. 1–6, 2022, doi: 10.1587/elex.19.20210538.

[3] J. R. Jalos and S. J. E. Delgado, "Bandgap voltage reference analysis using LTspice XVII," presented at the 29th ASEMEP National Technical Symposium, Batangas State University, Batangas, Philippines.

[4] J. Zhou, X. Xin, and J. Ren, "Design of a bandgap reference voltage source with low temperature coefficient and high precision," *J. Phys.: Conf. Ser.*, vol. 2170, Art. no. 012029, 2022, doi: 10.1088/1742-6596/2170/1/012029.

[5] S. M. M. Shal, M. D. Rahimabad, and A. Heidari, "Design and simulation of a low voltage bandgap reference circuit in 0.18 µm CMOS technology for the supply range of 1.6 to 4.15 V," University of Guilan, Rasht, Iran, Jun. 11, 2025, doi: 10.21203/rs.3.rs-6831576/v1.

[6] A. Rahman, S. Kishore, and A. R. Abdul Rajak, "Design and study the performance of a CMOS-based ring oscillator architecture for 5G mobile communication," *Emerging Science Journal*, vol. 8, no. 1, pp. 283–296, Feb. 2024.

[7] S. Suman, K. G. Sharma, and P. K. Ghosh, "Analysis of phase noise and jitter in ring oscillators," *Innovative Systems Design and Engineering*, vol. 8, no. 2, pp. 1-9, 2017.

[8] M. Esmaeilzadeh, Y. Audet, M. Ali, and M. Sawan, "A low-phase-noise CMOS ring voltage-controlled oscillator intended for time-based sensor interfaces," *IEEE Access*, 2022, doi: 10.1109/ACCESS.2022.3208273.

[9] R. Udaiyakumar, S. Joseph, and T. V. P. Sundararajan, "Performance analysis in digital circuits for process corner variations, slew-rate and load capacitance," *Wireless Personal Communications*, vol. 103, pp. 99–115, 2018, doi: 10.1007/s11277-018-5428-8.

[10] N. Ramanjaneyulu, D. Satyanarayana, and K. Satya Prasad, "Design of a three stage ring VCO in 0.18 µm CMOS under PVT variations," *International Journal of Computer Applications*, vol. 170, no. 8, pp. 35–39, Jul. 2017.

[11] S. K. Dash, B. P. De, B. Appasani, and N. K. Rout, "Design of low power current starved ring oscillators using modified particle swarm optimization," *Facta Universitatis, Series: Electronics and Energetics*, vol. 38, no. 4, pp. 625–637, Dec. 2025, doi: 10.2298/FUEE2504625D.

[12] R. Ahirwar, M. Pattanaik, and P. Srivastava, "Radiation hardened by design-based voltage controlled oscillator for low power phase locked loop application," *Journal of Electronic Testing*, vol. 40, no. 2, pp. 171-184, Apr. 2024, doi: 10.1007/s10836-024-06113-x.

[13] R. Arya and B. K. Singh, "45-nm CMOS ring oscillator," presented at the *1st International Conference on Intelligent Computation and Analytics on Sustainable Energy and Environment*, Ghani Khan Choudhury Institute of Engineering and Technology, Malda, West Bengal, India, Sep. 21–23, 2023.

[14] M. A. Abdullah, M. B. Elamien, and M. J. Deen, "0.4 V CMOS current-controlled tunable ring oscillator for low-power IoT and biomedical applications," *Electronics*, vol. 14, Art. no. 2209, pp. 1–15, 2025, doi: 10.3390/electronics14112209.

[15] Y. Cheng, M. Chan, K. Hui, M.-C. Jeng, Z. Liu, J. Huang, K. Chen, J. Chen, R. Tu, P. K. Ko, and C. Hu, *BSIM3v3 Manual (Final Version)*, Memorandum No. UCB/ERL M97/2. Berkeley, CA, USA: Electronics Research Laboratory, College of Engineering, University of California, Berkeley, Jan. 13, 1997.

[16] A. O.-O. Esho, T. D. Iluyomade, T. M. Olatunde, and O. P. Igbinenikaro, "A comprehensive review of energy-efficient design in satellite communication systems," *International Journal of Engineering Research Updates*, vol. 6, no. 2, pp. 13–25, 2024, doi: 10.53430/ijeru.2024.6.2.0024.

[17] National Communications Commission, *Personal Locator Beacon Technical Specifications*. Jul. 15, 2020.

[18] C. Nieto-Peroy and M. R. Emami, "CubeSat mission: From design to operation," *Applied Sciences*, vol. 9, no. 15, Art. no. 3110, 2019.

[19] N. Zosimovych, "Communication system for nanosatellite earth observation," *Advances in Aerospace Science and Technology*, vol. 6, no. 3, pp. 134–157, 2021.

[20] A. C. Salces, M. P. Sejera, S. Kim, H. Masui, M. Cho, "Development and investigation of communication issues on a CubeSat-onboard amateur radio payload with APRS digipeater and store-and-forward capabilities," *UNISEC Space Takumi Journal for Practical Study of Problem Finding and Solving in Space Systems*, vol. 9, no. 2, pp. 17–46, 2020.



Thit Waso Khine received her B.E. (Electronics) Degree from Mandalay Technological University in 2003, and M.E. (Electronics) Degree from Mandalay Technological University in 2006, respectively. She is an Associate Professor of the Department of Electronic Engineering at Technological University (Taunggyi) and she is also now a PhD (Plan B) candidate at the Department of Electronic Engineering of Yangon Technological University. (email: thitwasokhine@gmail.com).



Dr. Lei Lei Yin Win is a Professor and Head of the Department of Electronic Engineering at Yangon Technological University. (email: maleileiyinwin.ytu@gmail.com).



Dr. Khin Kyu Kyu Win is a Professor of the Department of Electronic Engineering at Yangon Technological University. (email: khinkyukyuwin.ytu@gmail.com).



Dr. Ei Ei Khin is a Professor of the Department of Electronic Engineering at Yangon Technological University. She also manages the Remote Sensing and GIS Research Centre of YTU. (email: maeieikhin.ytu@gmail.com).



Dr. Mya Mya Aye is an Associate Professor of the Department of Electronic Engineering at Yangon Technological University. (email: mamyamyaaye.ytu@gmail.com).